eMemory Introduction .

ememory

IPR Notice

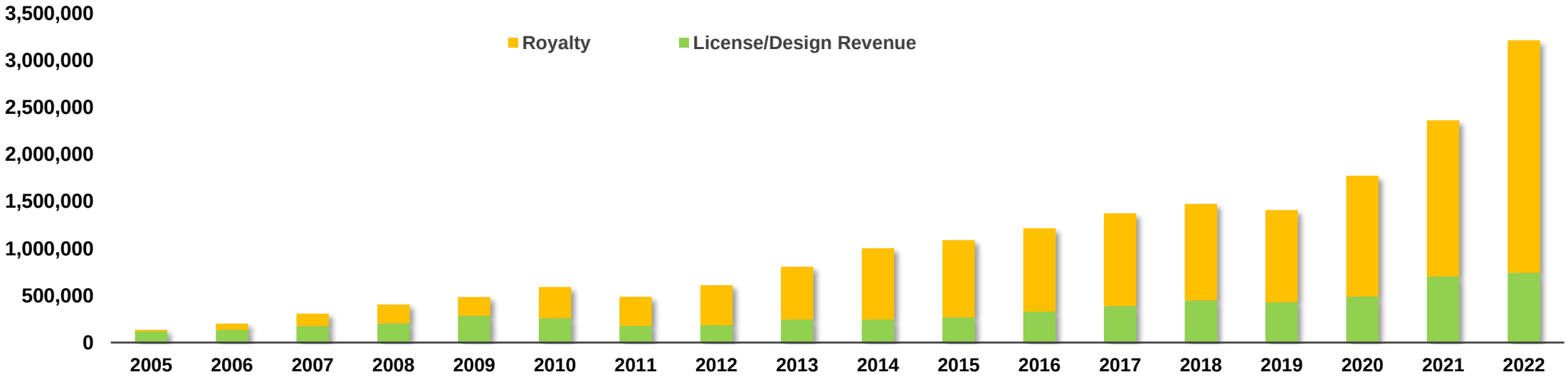
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Company Overview

- eMemory is the global leader of embedded non-volatile memory IP

Revenue Trend

(Unit: NT$ 1,000)



Founded
In 2000

Based in Hsinchu, Taiwan. IPO in 2011. Over 50M wafers shipped.

1100+
Patents Issued

199 pending patents. 334 employees with 67% R&D personnel.

Best IP Partner
With TSMC

TSMC Best IP Partner Award since 2010.

Technology Portfolio



With access to eMemory's widely verified IP process platform, PUFsecurity is uniquely positioned to provide **OTP and PUF-based** Security IP Solutions with **extensive availability** across various foundries and process nodes.

PUFsecurity

PUF-based Security IP Design & Service

- **PUF**se
- **PUF**cc
- **PUF**rt

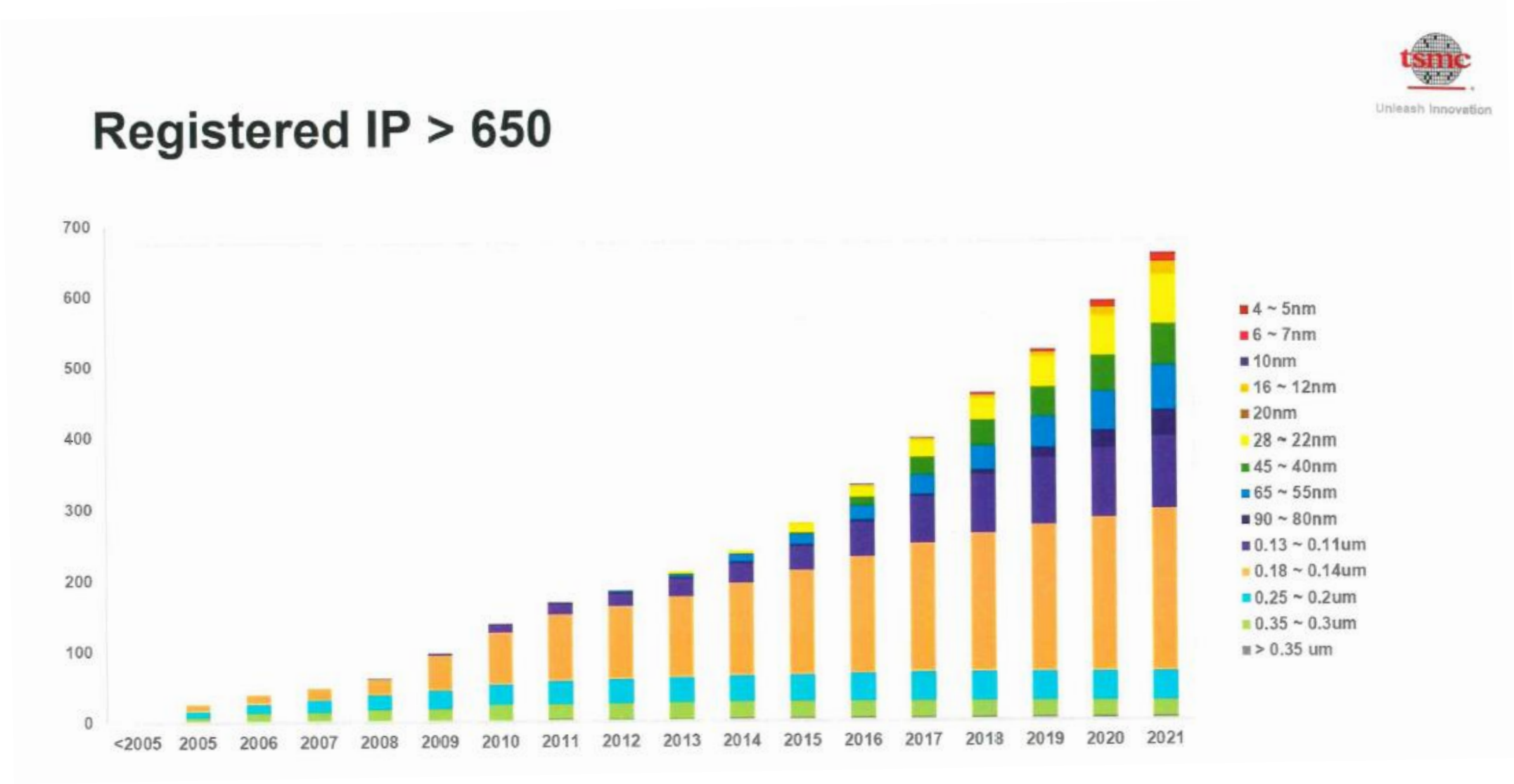
eMemory

Technology Provider + IP Design & Service

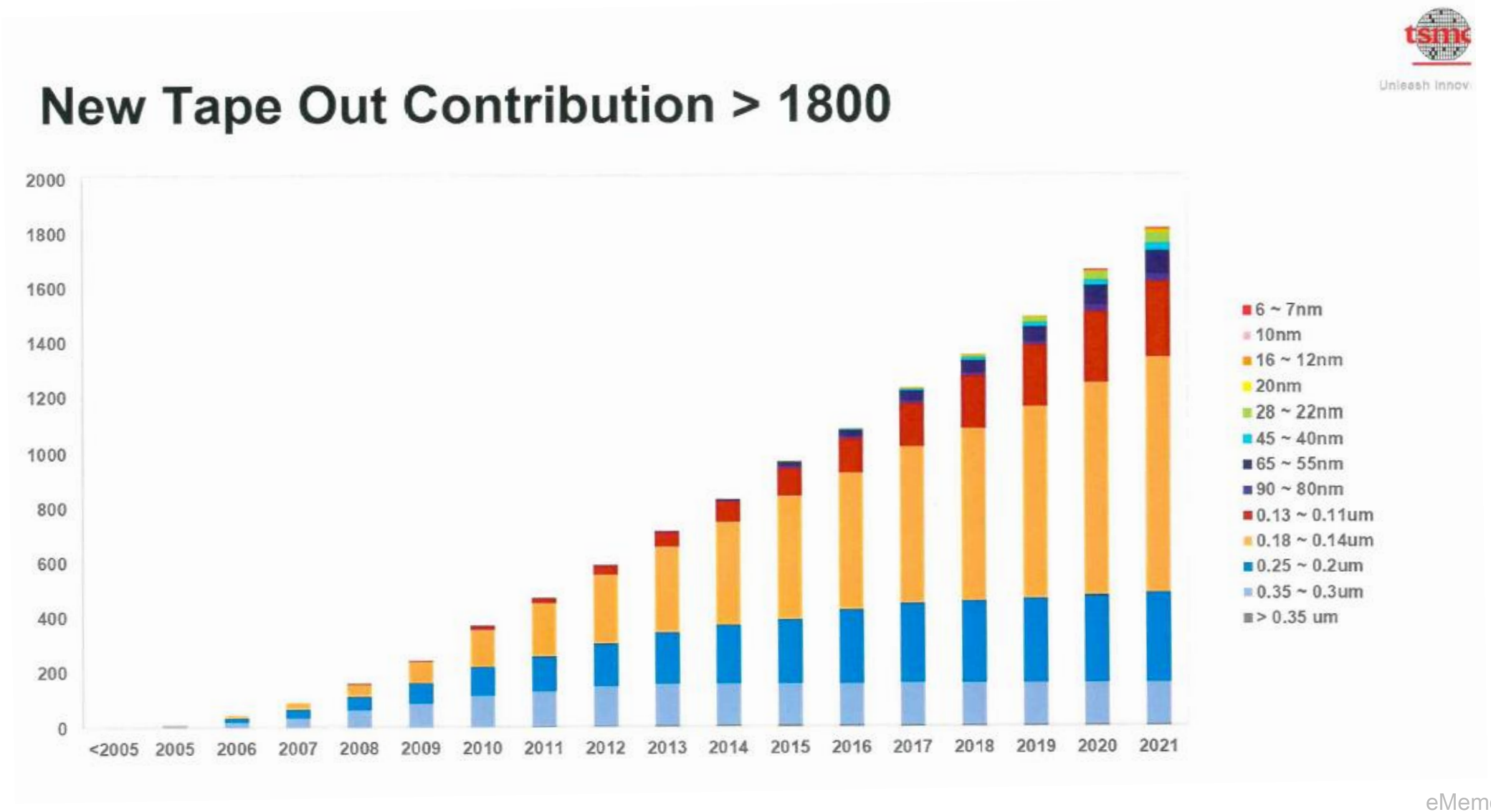
- **NeoPUF (PUF)**
- **NeoFuse (OTP)**
- NeoEE (MTP)
- NeoFlash
- NeoMTP (MTP)
- **NeoBit (OTP)**

2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024

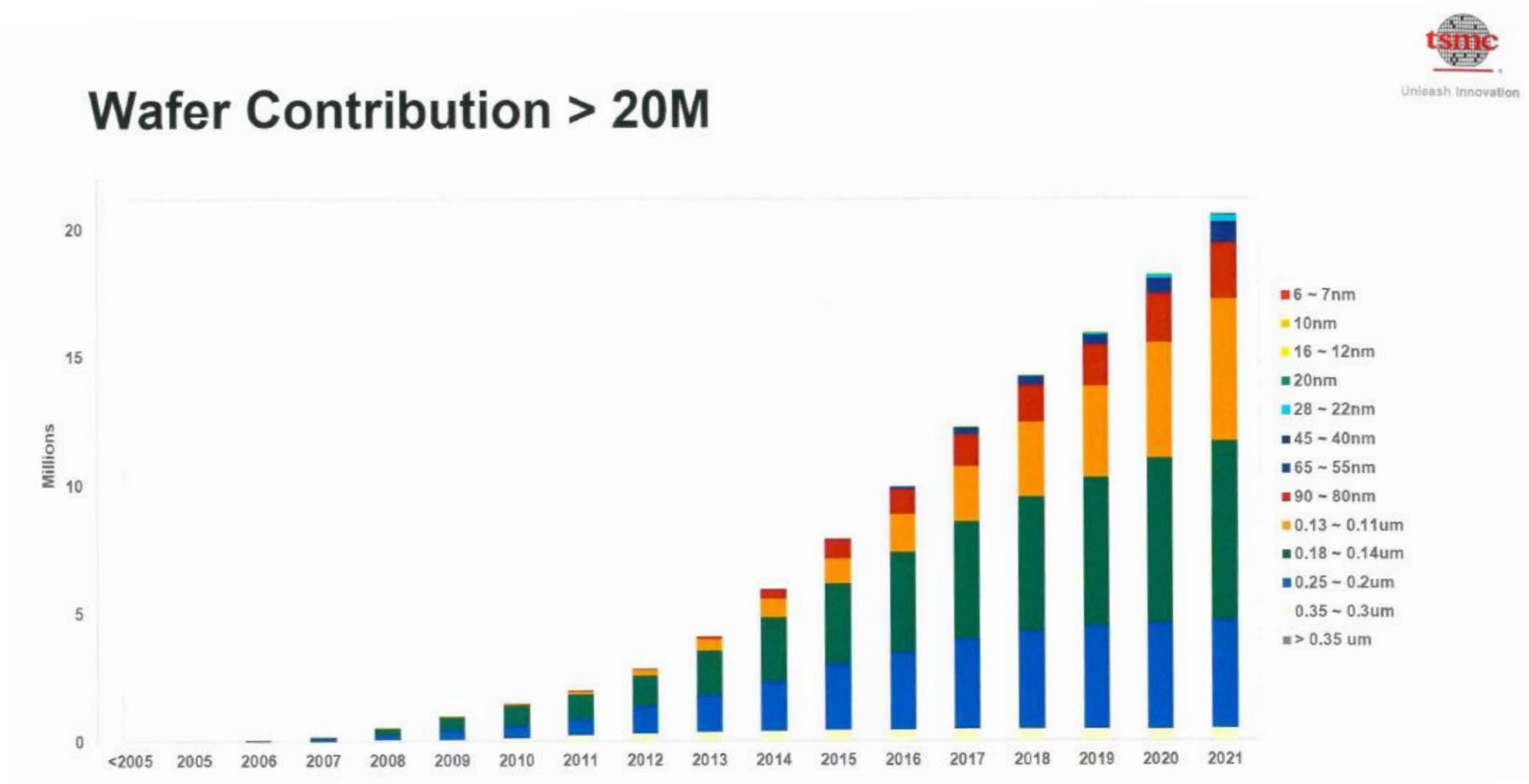
Registered IPs at TSMC



NTOs at TSMC


New Tape Out Contribution > 1800
2000
1800
1600
1400
1200
1000
800
600
400
200
0
<2005
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
6 ~ 7nm
10nm
16 ~ 12nm
20nm
28 ~ 22nm
45 ~ 40nm
65 ~ 55nm
90 ~ 80nm
0.13 ~ 0.11um
0.18 ~ 0.14um
0.25 ~ 0.2um
0.35 ~ 0.3um
> 0.35 um

Wafer Contribution at TSMC



Revenue and Tape-out by Technology

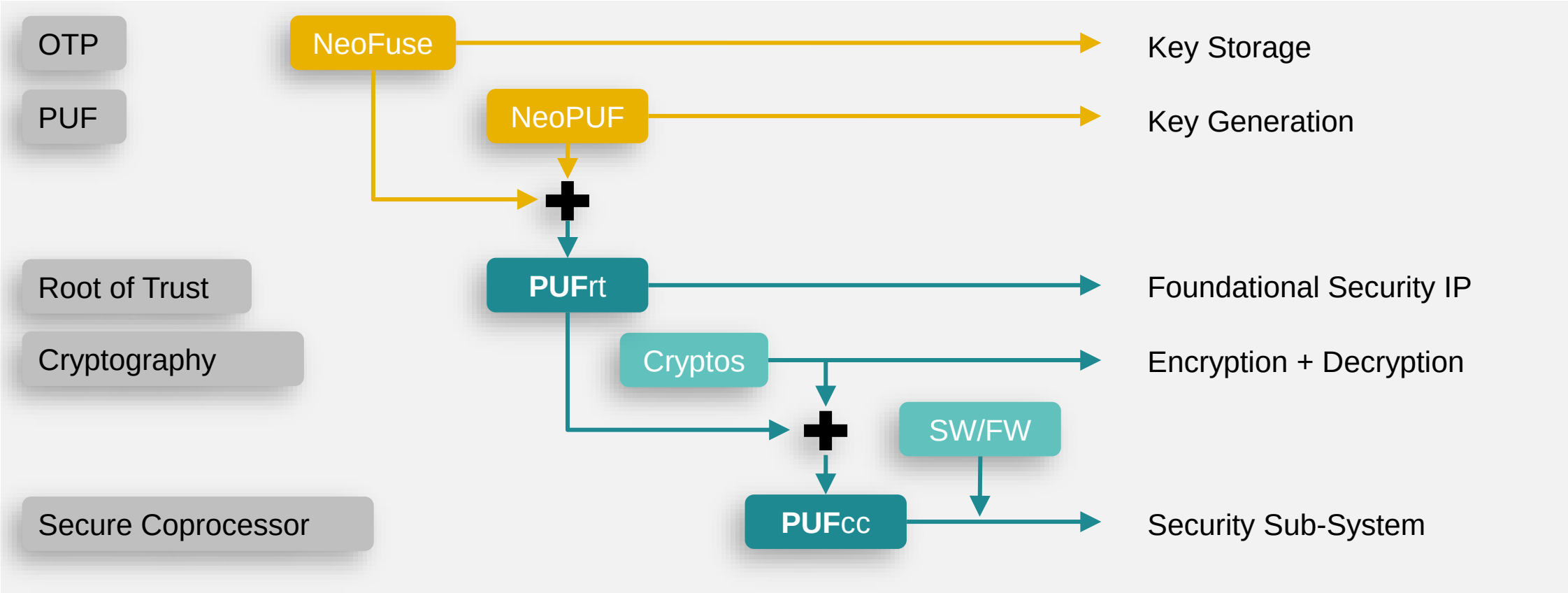
	NTO		Revenue (USD)		
Year	**NeoBit**	**NeoFuse**	**NeoBit**	**NeoFuse**	**PUF-based**
2002	3				
2003	28				
2004	39				
2005	68		$ 4,217,380		
2006	133		$ 6,202,270		
2007	220		$ 9,402,479		
2008	253		$ 12,896,211		
2009	268		$ 11,695,587		
2010	285		$ 15,873,331		
2011	254		$ 15,399,098		
2012	271		$ 19,620,768		
2013	369	1	$ 25,436,669	$ 382,084	
2014	373	3	$ 31,831,985	$ 328,787	
2015	314	11	$ 30,943,426	$ 1,080,373	
2016	273	30	$ 30,247,340	$ 3,636,142	
2017	257	61	$ 34,619,653	$ 5,238,351	
2018	254	87	$ 31,834,860	$ 10,773,223	$ 85,000
2019	227	110	$ 27,602,332	$ 14,466,279	$ 195,000
2020	249	185	$ 30,378,346	$ 26,437,660	$ 434,998
2021	255	264	$ 32,367,560	$ 44,011,223	$ 1,160,702
2022	274	243	$ 35,327,060	$ 63,762,480	$ 4,207,209
Total	**4,667**	**995**	**$ 405,896,355**	**$ 170,116,602**	**$ 6,082,909**

*NTO stands for **New Tape-Out**

* Revenue includes both **licensing** and **royalty**

Evolution from OTP to Security Sub-Systems

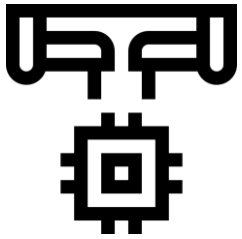
- Based on OTP Technologies, many different security functions IPs have evolved
- Regulations, such as TPM 2.0, now require Hardware Root of Trust



Security Business Development

- As eMemory is an established IP company, there are different **platforms** that we can leverage for sales in security IPs and sub-systems

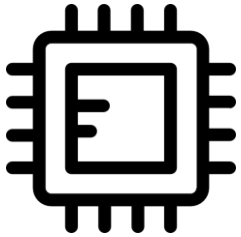
Foundry Platforms



TSMC, Intel, UMC, GF, etc.

- Licensed our security technology to major foundries
- Co-promotional activities

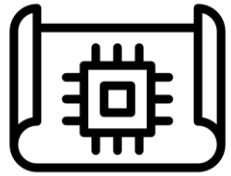
CPU Partners



Arm, RISC-V, Cadence, etc.

- SoC customers looking for both CPU and security subsystems

CSP



More to come

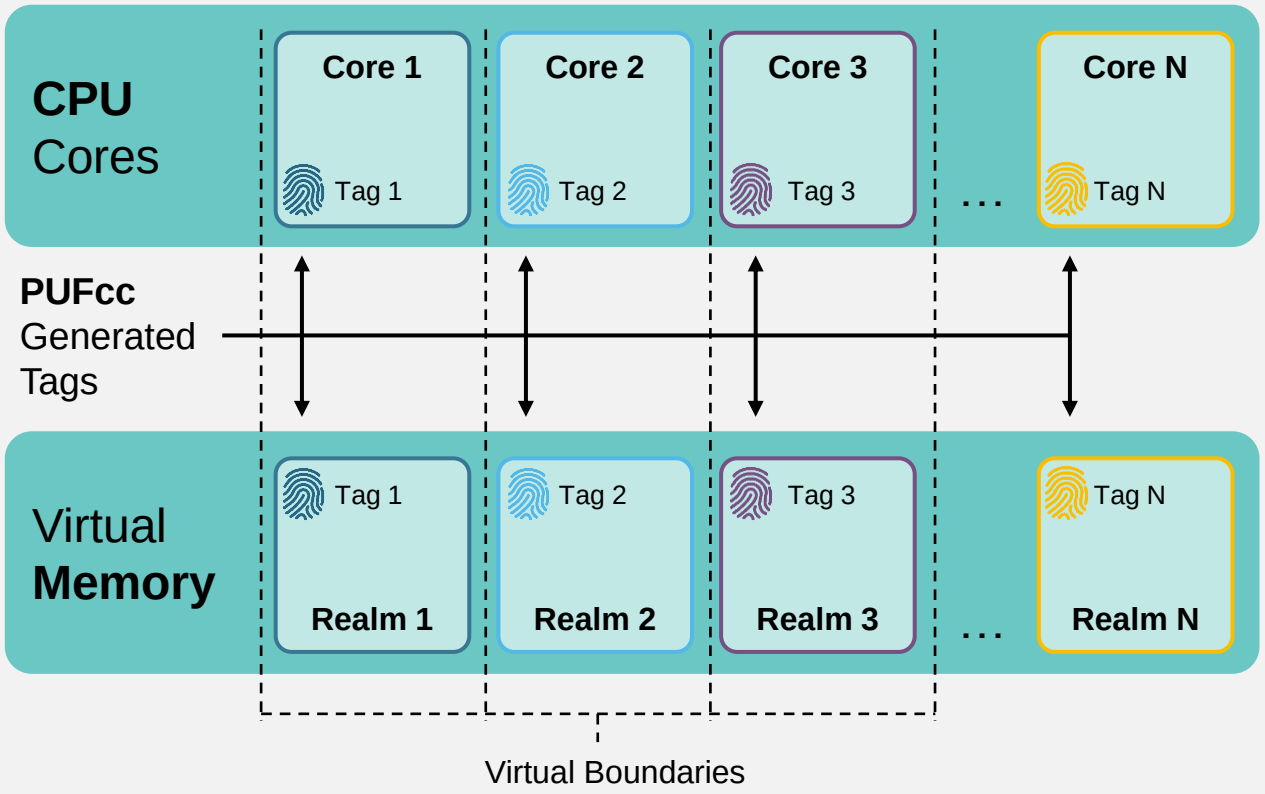
- Work with CSP and system companies for embedded security on a chip level

Market **Application**

- Customers with many different applications will begin to adopt **PUF-based Security Solutions**

CPU	AI	SSD
DPU	DTV/STB	Wi-Fi
FPGA	ISP	And More.

Next Computing: **Confidential Computing**

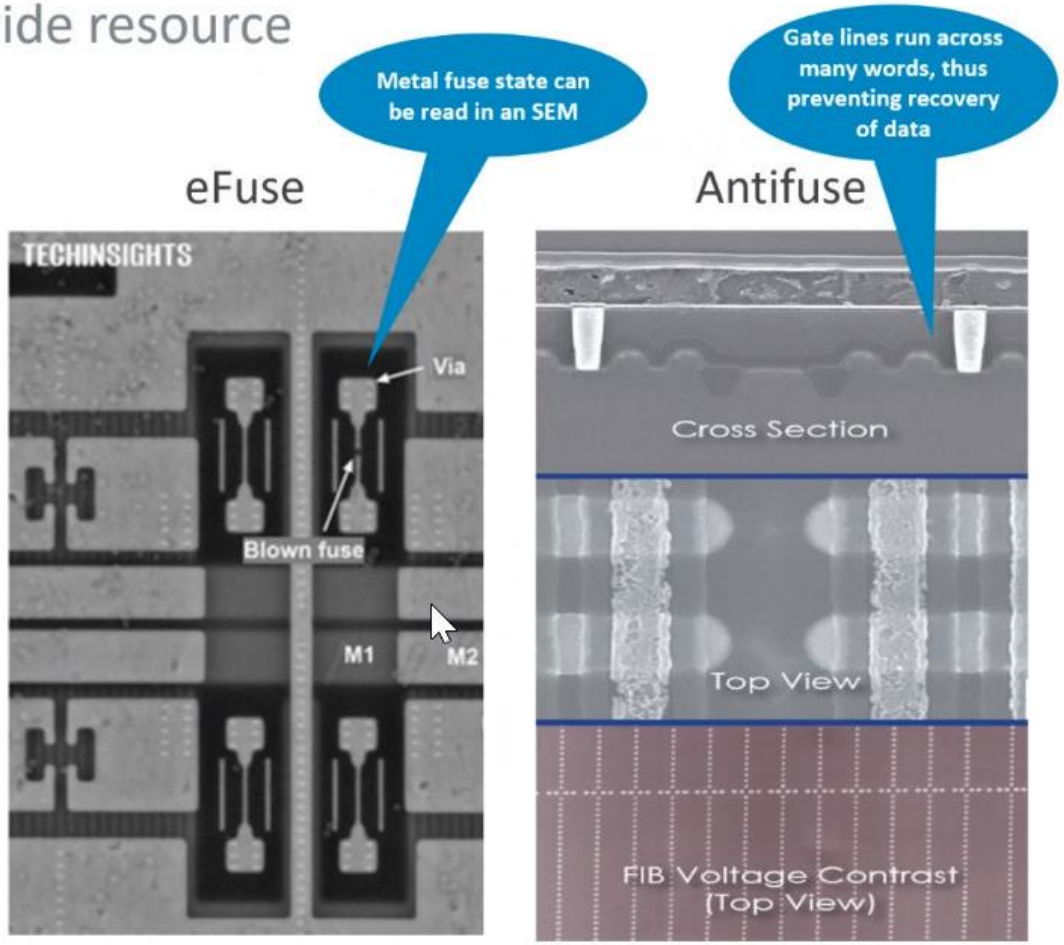


- **Protect data** in the Virtual Memory of Multi-Core CPUs
- CPU Cores and Virtual Memory have unique corresponding **tag numbers**
- Tag numbers are internally **randomly generated** by **PUFcc** (Crypto Coprocessor IP)

Runtime **Security** Architecture **OTP**

One Time Programable (OTP) memory is a SoC-wide resource

- RSS supports OTP as field-programmable to store confidential code and data
- eFuse:
  - Area efficient for smaller arrays
  - Typically not field programmable
  - Can be easily read by delayering SoC (a few $k cost)
    - The secure channel key can be compromised
    - The device can then be cloned
- Antifuse OTP:
  - Cannot be read using a scanning electron microscope
  - Dense bit cells, efficient for large arrays
    - Macro periphery is large versus eFuse
  - Integrated charge pump enables field programming
  - PUF can be included for a small additional area
    - ~0.04mm2 on 7nm for 128x32 bit PUF

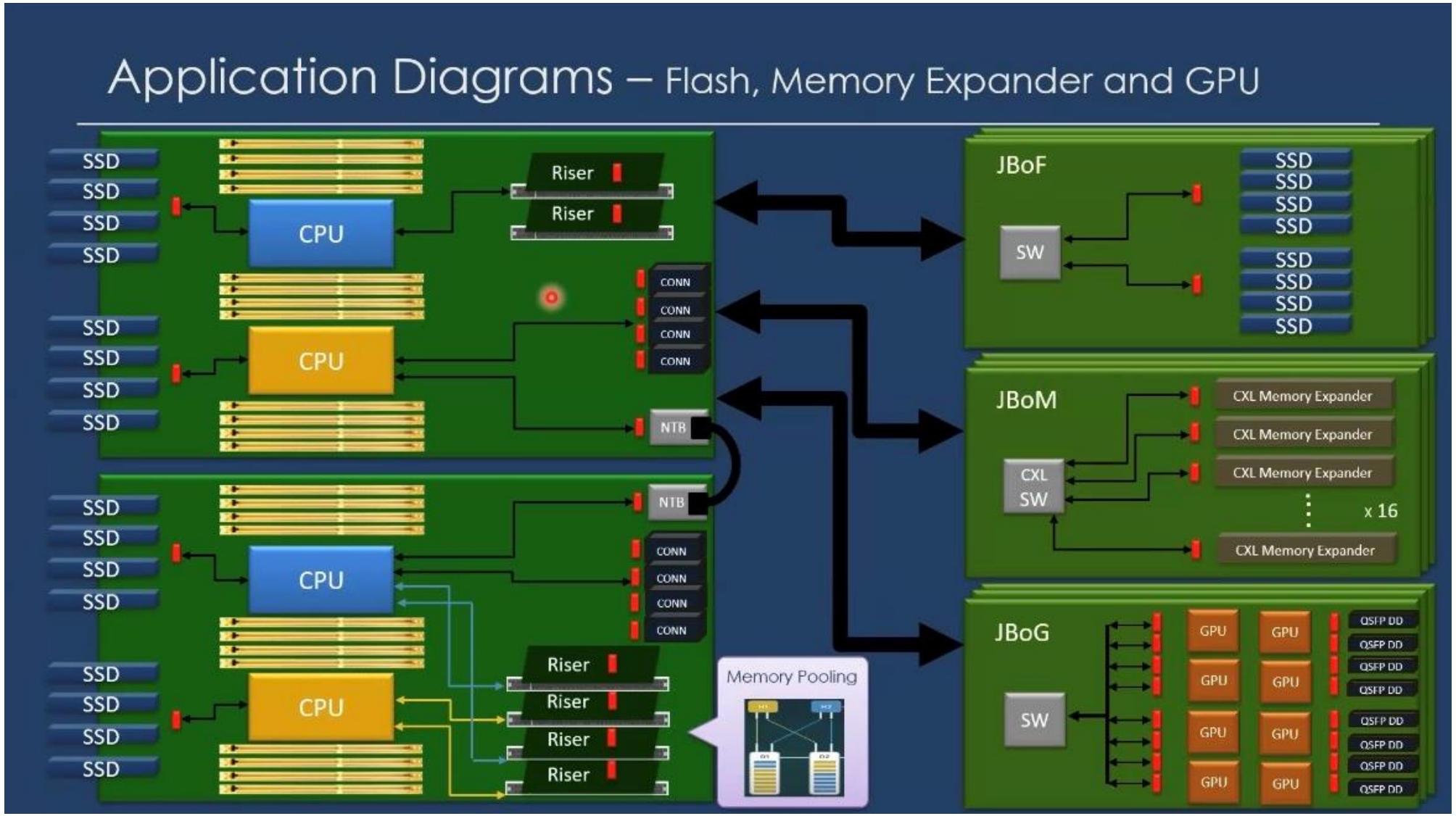


https://semiengineering.com/the-benefits-of-antifuse-otp/

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AI Server Architecture



Thank You for your time .

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eMemory Website: https://www.ememory.com.tw/
PUFsecurity Website: https://www.pufsecurity.com/